3DV-E - AN EMBEDDED, DENSE STEROVISION-BASED SYSTEM

Camellini G. - VisLab, Università di Parma
cgabri@vislab.it

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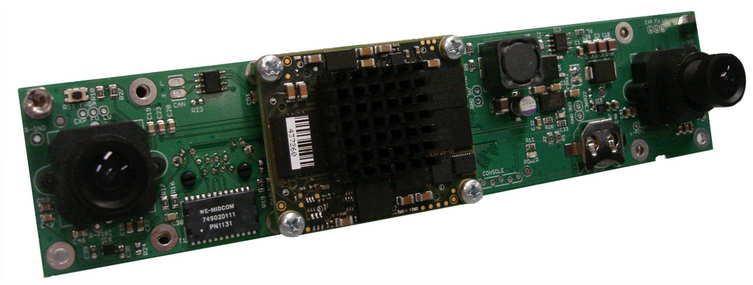
Abstract

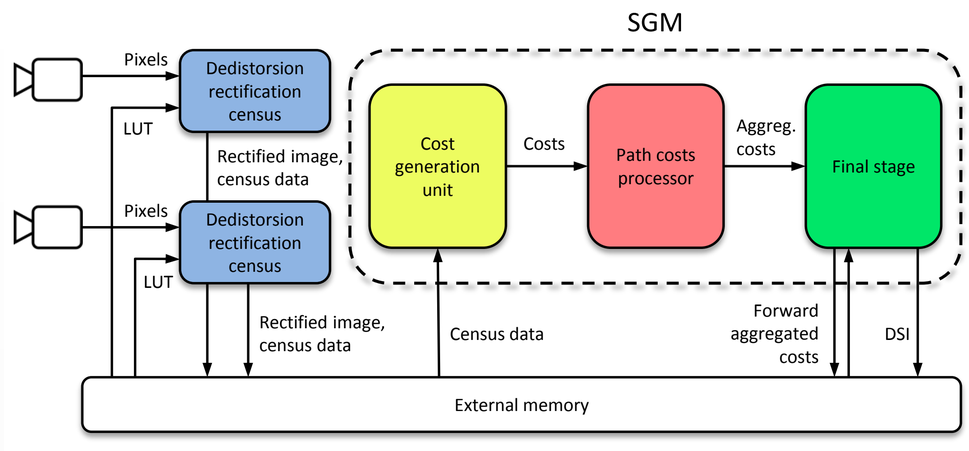
This poster describes an embedded, low-cost and low-power dense stereo reconstruction system, running at 27fps at VGA resolution. The processing pipeline includes an image rectification stage, a cost generation unit based on the census transform, a Semi-Global cost optimization stage, and a final minimization step. The hardware is based on a Xilinx Zynq™ System-on-Chip, which provides a FPGA and a physical dual-core ARM CPU for control and streaming.

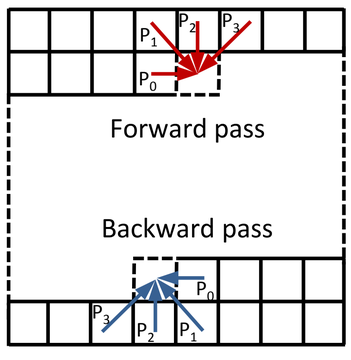
System overview

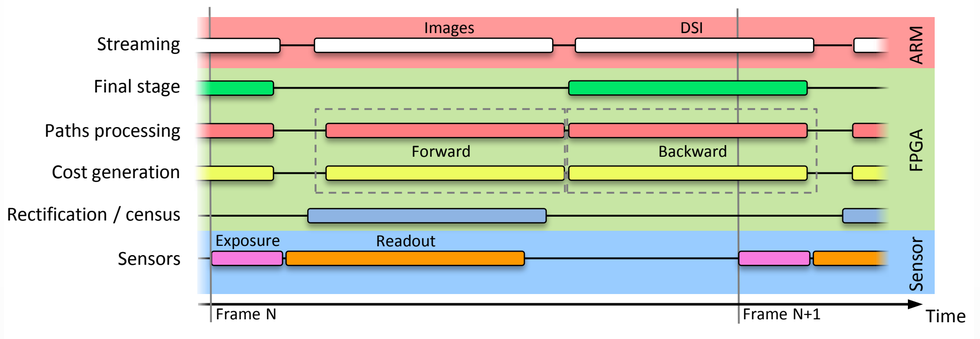


- 640 x 480 pixel @ 27fps (low latency) stereo rectification and disparity computation
- Disparity computation alghoritm:
  Census Transform + Semi Global Matching (8 paths) + Minimization
- Based on Xilinx ZYNQ-7020 SoC (FPGA + dual core ARM Cortex-A9)
- GigabitEthernet output (raw/rectified L&R, dispariy images); Low power (5W); Trigger and general purpose I/O; Gyro+accelerometer; High-level tasks capability

System Architecture

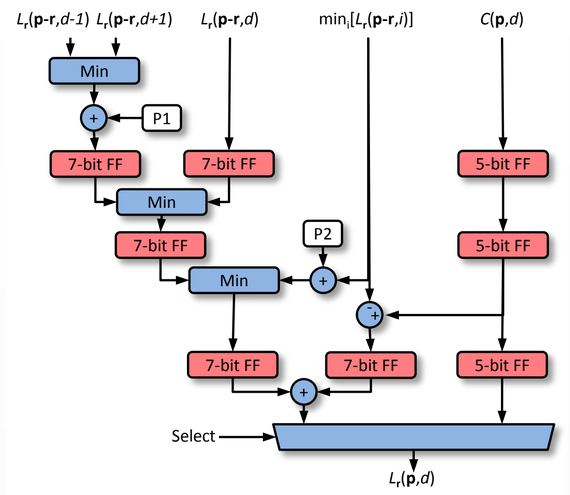






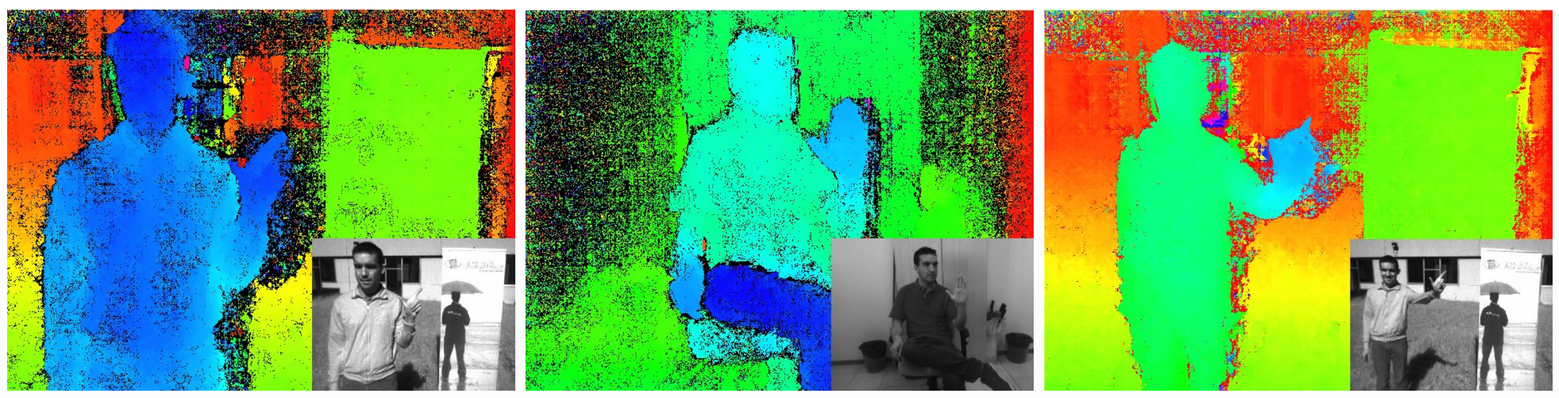
Left and right figures illustrate the stereo reconstruction pipeline: first step involves dedistortion and rectification on pixels captured by sensors, followed by census tranform used in SGM to generate initial costs cube. The Semi-Global matching approximates the optimal solution by aggregate costs along 8 paths. This operation is splitted in forward ($0°$, $45°$, $90°$, $135°$) and backward ($180°$, $225°$, $270°$, $315°$) phases to reuse the same hardware resources (central figure). Finally minimization and noise suppression stage generates disparity image. Right image shows which units are active during the processing of one frame; high degree of parallelism is achieved between the units.

An Implementation Detail



Implementation of the elementary block for path costs computation in SGM.

Outputs & Results



Implementation	Hardware platform	Time [ms]	Disp. Rate 10^6/s	Implementation	Hardware platform	Time [ms]	Disp. Rate 10^6/s
Gehrig ECVW10	CPU i7 @3.3GHz	224	117	Banz ICCV11	GPU Tesla C2050	16	2457
Broggi IROS11	CPU i7 @3.2GHz	27	970	Gehrig ICVS09	FPGA Virtex4	40	218
Hirschmuller ISVC10	GPU Gforce 8800	238	165	Banz SAMOS10	FPGA Virtex5	9.7	4053
Nedevschi IV10	GPU Gforce GTX	19	578	**this system**	**SoC ZYNQ 7020**	**33**	**1192**

Acknowledge

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References

[1] G. Camellini, M. Felisa, P. Medici and P. Zani, F. Gregoretti, C. Passerone, R. Passerone
3DV – An Embedded, Dense Stereovision-based Depth Mapping System,
in *2014 IEEE Intelligent Vehicles Symposium*, 2014

[2] 3DV-E details & demos: `http://www.ce.unipr.it/people/cgabri/icvss2014.html`